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(54) Abstract Title
Phase locked loop for high frequency signals

(57) With a PLL circuit according to the invention, the precharge function necessary for setting a required initial state of the VCO 2 is achieved by means of an additional precharge pump 12 inserted in parallel to the main charge pump 9 or alternatively (fig.6 not shown) by means of multiplexers implemented directly with the main charge pump 9. In both cases, the control of the precharge function takes place by means of two control signals pd, pcp. One logic control signal pcp ensures that during the precharge, the PLL is in the standby mode and the precharge pump is in the active state and after the precharge, the PLL is in the active mode and the precharge pump is in the passive mode. The other voltage pd ensures that the precharge pump applies to the VCO the control voltage necessary for required initial state to facilitate rapid locking. Applications may be in GSM, PCN, PCS receivers. The PLL may include a quadrature modulator after the filter 3.

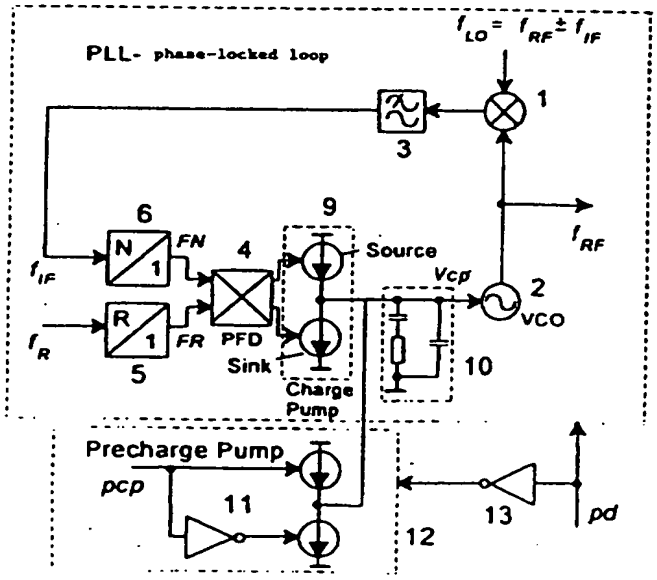

FIG. 4

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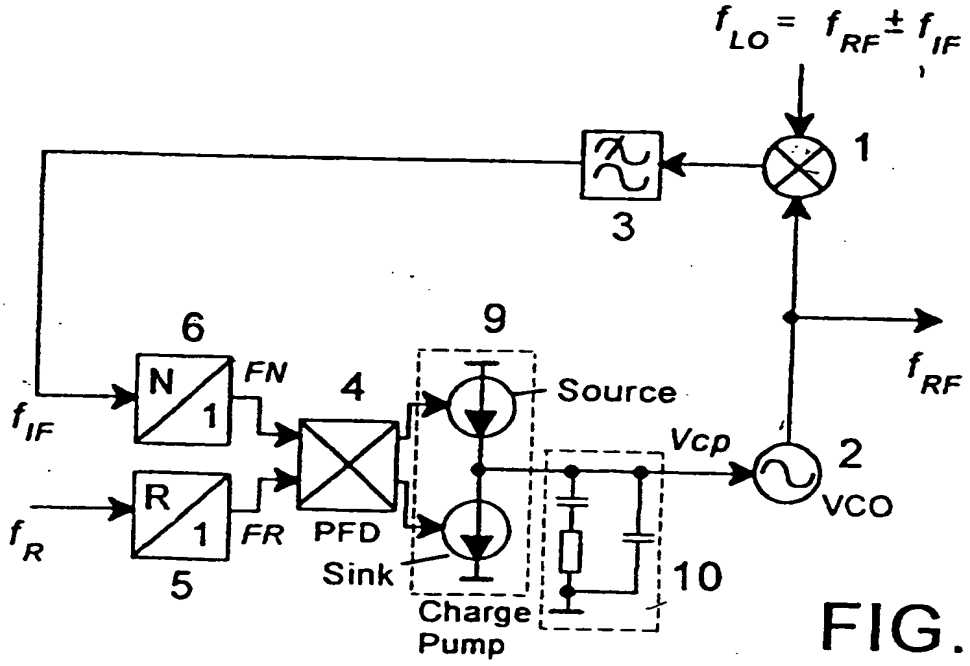

FIG. 1

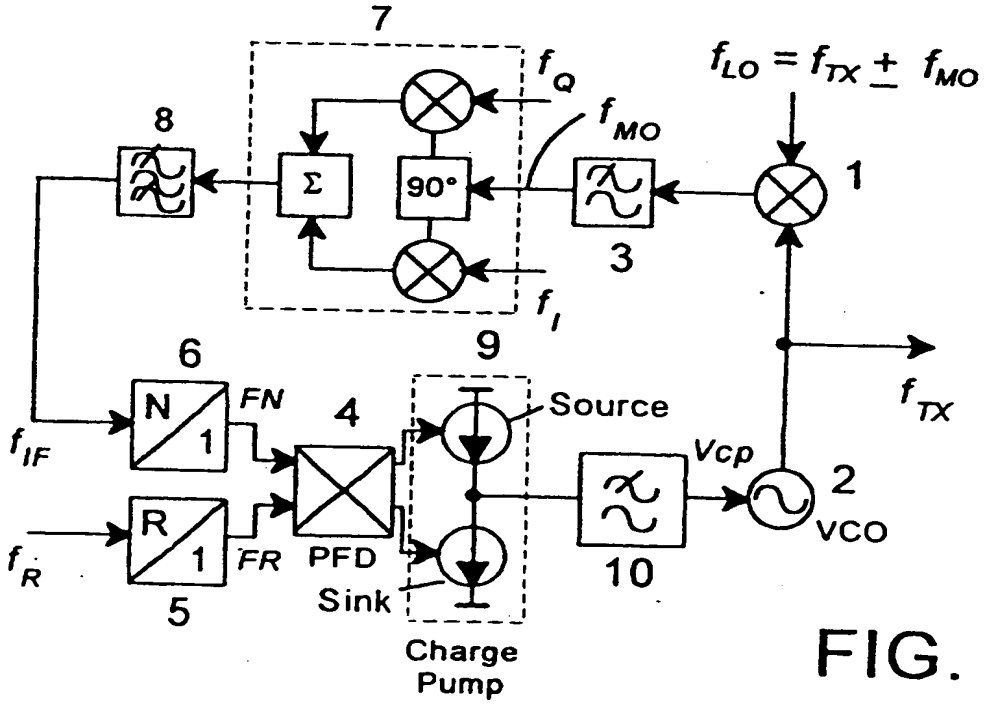

FIG. 2

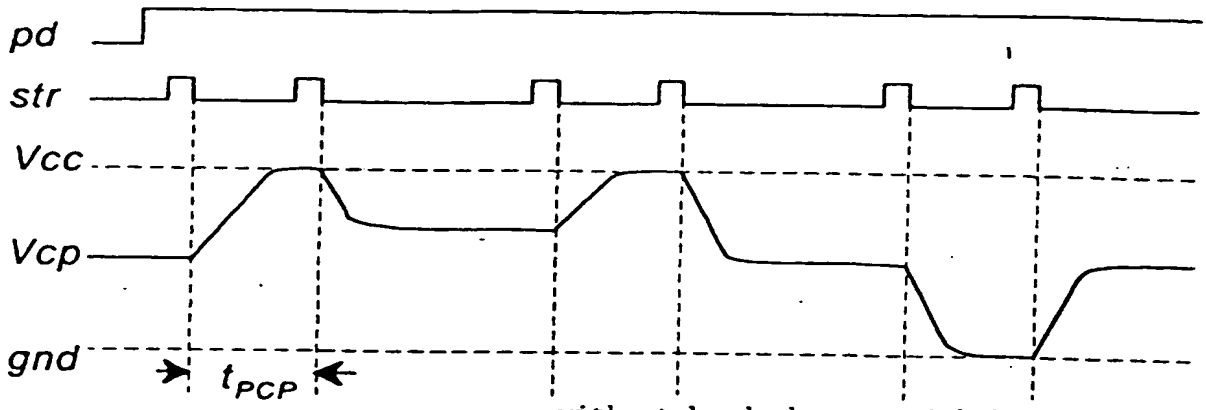

FIG. 3

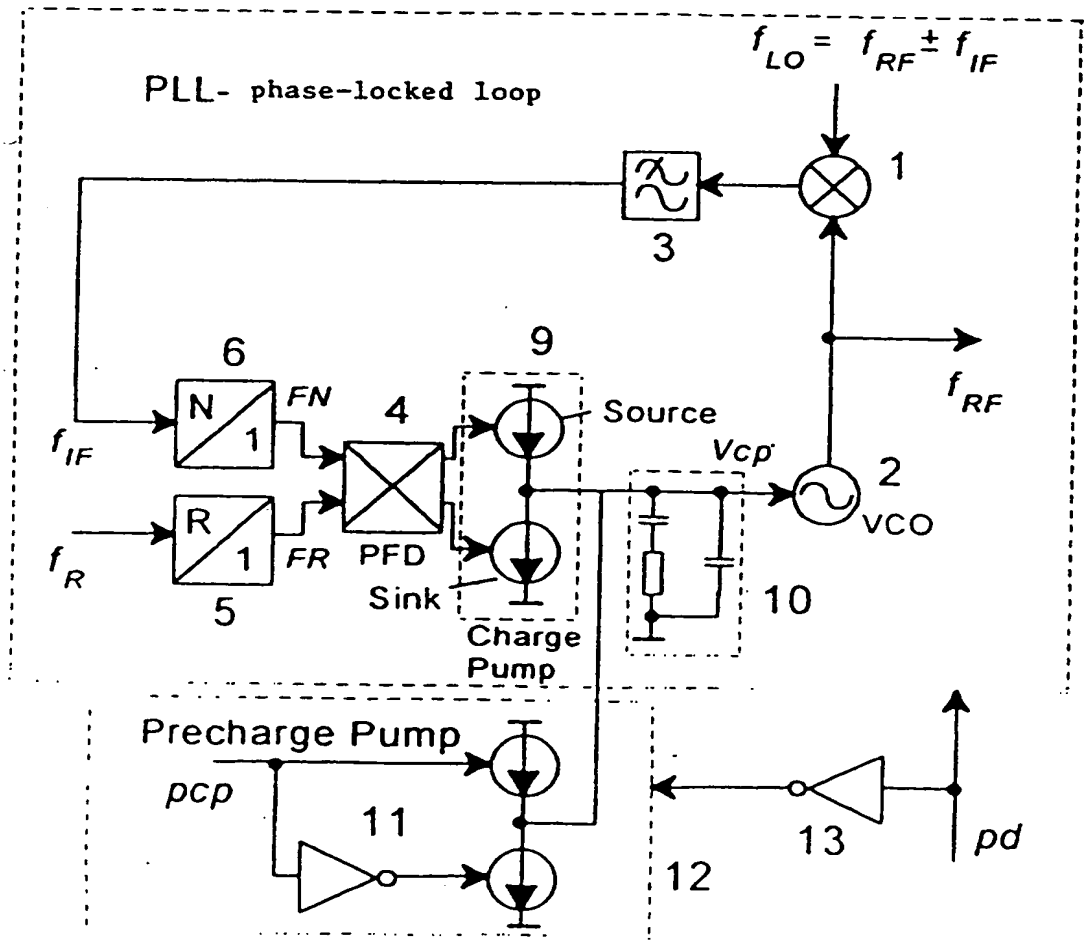

FIG. 4

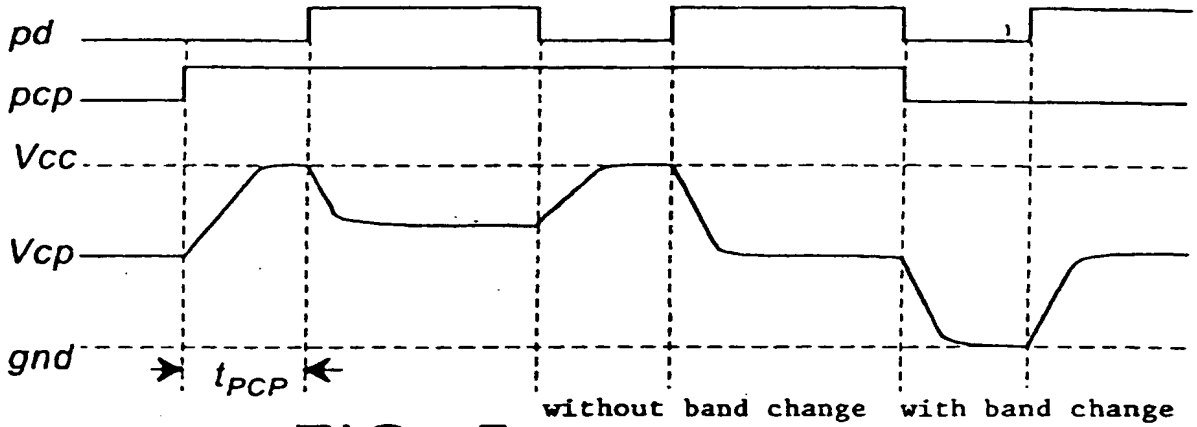

FIG. 5

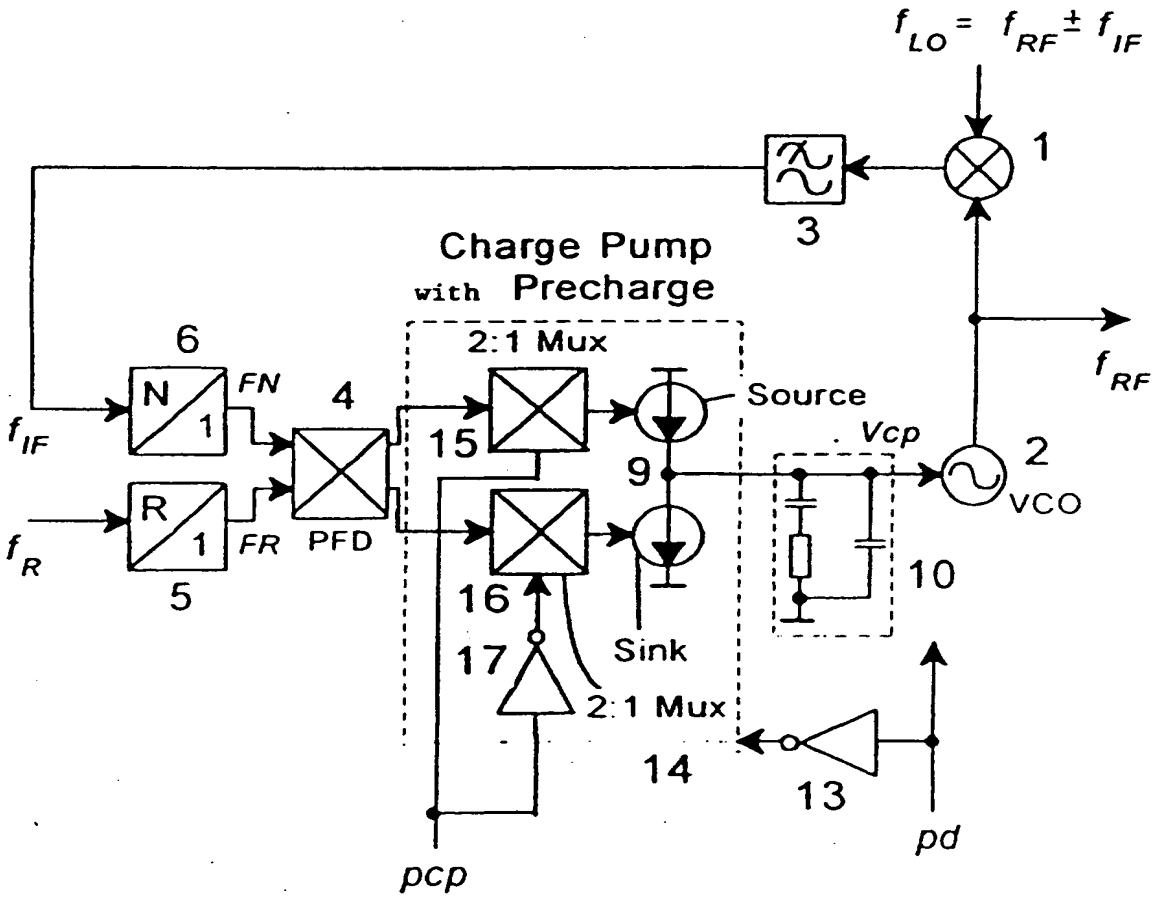

FIG. 6

PHASE-LOCKED LOOP (PLL) FOR HIGH-FREQUENCY (HF) SIGNALS

The invention relates to a phase-locked loop (PLL) for high-frequency (HF) signals.

Various HF switching circuits with phase-locked loop (PLL), which can be implemented as integrated circuits (ICs) in currently available semiconductor technology, have been developed for telecommunications systems. Figures 1 and 2 show two examples of such known HF switching circuits.

The example shown in Figure 1 is a PLL frequency synthesizer with a loop mixer (MPLL) and the example shown in Figure 2 is an upconversion modulation loop transmitter (UML-TX), with the local signal f_{LO} and the reference signal f_R being generated by an oscillator or frequency synthesizer.

The loop mixer 1 is used in both examples for the downward mixing of the output frequency of a voltage-controlled oscillator (VCO) 2. Undesirable mixed products of the loop mixer 1 are suppressed by a passive low-pass filter 3.

The phase-locked loop (PLL) has a phase-frequency detector (PFD) 4 to which is supplied, as the first of two input signals, a reference signal with the frequency f_R (before the frequency division), controlled by way of a frequency divider 5 with the divider ratio R/1. A signal with the frequency f_{IF} (before frequency division), is supplied to the phase-frequency detector as the second input signal, controlled by way of a frequency divider 6 with a divider ratio of N/1. The signal with the frequency f_{IF} is derived from the output signal of the voltage-controlled oscillator (VCO) 2 with the frequency f_{RF} (Figure 1) or the transmitting frequency f_{TX} (Figure 2) subject to mixing in the loop mixer 1 with a frequency synthesizer signal or local oscillator signal f_{LO} and in the case of Figure 2 another modulation in a quadrature modulator 7 and a

filtering in a passive band-pass filter 8.

The output signals of the phase-frequency detector 4 present at two outputs are supplied to the two inputs of a charge pump 9 having two current sources (source and sink). The control voltage Vcp is output from the charge pump and is supplied by way of a passive loop low-pass filter 10 to control the voltage-controlled oscillator 2.

The known phase-locked loops (PLL) of this kind are mostly programmed with the aid of a bus, for example with a 3-line bus, in their standby mode (only bus active). After the programming, the locked loops are switched from the standby mode into the active mode. During the transient phase after the connection the phase-locked loop (PLL) forces the voltage-controlled oscillator (VCO) 2 to follow the reference signal f_R in such a way that phase angles and frequency positions of the two input signals at the phase-frequency detector 4 remain the same after the "lock-in" has taken place.

In the development of the phase-locked loops (PLL), both single-band and dual-band applications are considered. With single-band cellular systems for GSM (Global System for Mobile Communications), PCN (Personal Communication Network) or PCS (Personal Communication System/Service) receivers and transmitters with the PLL phase-locked loops are only assembled for a corresponding frequency band.

With dual-band systems, operating frequencies of the receivers and transmitters are changed over, for example between GSM and PCN bands or between GSM and PCS bands, i.e. band changes take place here. If the local frequency $f_{LO} = f_{RF} + f_{IF}$ with GSM (f_{RF} = 900 MHz) and $f_{LO} = f_{RF} - f_{IF}$ with PCN and PCS (f_{RF} = 1800 MHz or 1900 MHz) is selected for dual-band systems, this frequency lies between the two frequency bands between

which there is to be a changeover.

For this reason, only a small frequency band range of the frequency synthesizer generating the local frequency f_{LO} is necessary, whereby the implementation of this frequency synthesizer with a low phase jitter and a short transient reaction is facilitated. During the transient phase the output frequency of the voltage-controlled oscillator (VCO) is to be controlled in such a way that a low frequency is produced at the output of the loop mixer. This necessary initial condition for a rapid "lock-in" of the PLL phase-locked loops arises for the following reasons.

With the MPLL and UML-TX:

1) the sensitivity of the N/1-divider 6 decreases at high frequencies;

2) the output power of the loop mixer 1 decreases at high frequencies;

3) the pass damping of the low-pass filter 3 increases at high frequencies.

In addition, with the UML-TX the following applies:

4) the sensitivity of the modulator 7 decreases at high frequencies;

5) the output power of the modulator 7 decreases at high frequencies;

6) the pass damping of the band-pass filter 8 increases at high frequencies.

The initial condition mentioned above for a rapid "lock-in" of the PLL phase-locked loop can be fulfilled with known PLL designs by the changeover of the polarity of the phase-frequency detector (PFD) 4. The changeover of the polarity takes place by means of software programming, for example by means of a 3 line bus.

With a positive polarity at the output of the phase-frequency detector 4 the current source "source"

in the charge pump 9 is connected if the FN signal compared with the FR signal is in phase or in frequency. With a negative polarity the current source "sink" of the charge pump 9 is connected. In order to fulfil the initial condition the PLL phase-locked loops must be controlled in the following way.

1) The R/1 and N/1 dividers 5 and 6, the phase-frequency detector 4 and the charge pump 9 are first of all connected, the voltage-controlled oscillator (VCO) 2 and the loop mixer 1 (and the modulator 7 with the UML-TX) remain disconnected, and the reference signal with the frequency f_r is applied to the input of the R/1 divider 5, whereas no signal is applied to the input of the N/1 divider 6.

2) The polarity of the phase-frequency detector 4 is changed over accordingly. In this way, the output voltage of the charge pump 9 Vcp = Vcc (supply direct voltage) with $f_{LO} = f_{RF} + f_{IF}$ for GSM or Vcp = gnd(0) with $f_{LO} = f_{RF} - f_{IF}$ for PCN and PCS is achieved.

3) The voltage-controlled oscillator (VCO) 2 and the loop mixer 1 (and the modulator 7 in the UML-TX) are connected after the precharge, and the entire PLL phase-locked loop is now in the active mode and operates with a low initial frequency at the output of the loop mixer 1.

The precharge is achieved with software programming, and so the term "software-precharge" is used for it. Figure 3 shows a simplified timing diagram of the "software-precharge" without and with band change. The period t_{PCP} from the changeover of the polarity of the phase-frequency detector 4 up to reaching the corresponding output voltage is called precharge time.

The signal pd is used for power-on (pd = high) and the signal str is used for bus-enable. In Figure 3 Vcc represents the supply direct voltage, Vcp the control

voltage for the voltage-controlled oscillator (VCO) and gnd the earth potential.

The hitherto-existing solution of the "software-precharge" has the following disadvantages.

1) There is a high power consumption during the precharge because the R/1 and N/1 dividers 5 and 6, the phase-frequency detector 4 and the charge pump 9 must be connected.

2) In the time frame and the time slots of TDMA (Time Division Multiple Access; time multiplex) cellular systems, for example GSM or PCN, where a time frame (4.616 ms) is divided into 8 time slots (577 μs), a critical timing of the trigger signals for the PLL phase-locked loops is produced because the connection of the switching circuits with two separate programming procedures (precharge and active) takes place by means of software.

3) The precharge is necessary both for single-band and for dual-band applications without band change because the PLL phase-locked loops during the disconnection have a non-defined voltage Vcp, in each case according to the output frequency of the voltage-controlled oscillator (VCO).

The invention seeks to provide for phase-locked loops (PLL) precharge design possibilities which manage with a lower power consumption during the precharge, which have an uncritical timing for the precharge and where for single-band and dual-band applications the programming procedure for the precharge is omitted, with the result that the PLL phase-locked loops can be connected more quickly.

According to a first aspect of the invention, there is provided a phase-locked loop for high-frequency signals with a phase-frequency detector to which there is supplied, as one input signal, a reference signal generated by way of frequency

division, as second input signal likewise generated by way of frequency division a signal derived from the output signal of a voltage-controlled oscillator and also subjected to a mixing with a local oscillator signal and optionally a modulation, and the output signals of which, after transmission by way of a charge pump device and a passive loop low-pass filter, are provided for controlling the voltage-controlled oscillator, wherein for setting (precharge) a certain initial state of the voltage-controlled oscillator, used for a rapid "lock-in", the charge pump device is controlled during the transient phase in such a way that it ensures the supply of the control voltage, respectively necessary for the initial state, at the voltage-controlled oscillator,

wherein the charge pump device, in addition to the charge pump, also contains a precharge pump which is activated by two logic control signals,

wherein the one logic control signal ensures that during the precharge the phase-locked loop is in the standby mode and only the precharge pump is in the active mode and after the precharge, conversely, the phase-locked loop is in the active mode and the precharge pump is in the standby mode, and wherein the other logic control signal ensures that the precharge pump applies to the voltage-controlled oscillator the control voltage respectively necessary for the initial state.

According to a second aspect of the present invention, there is provided a phase-locked loop for high-frequency signals with a phase-frequency detector to which there is supplied, as one input signal, a reference signal generated by way of frequency division, as second input signal likewise generated by way of frequency division a signal derived from the output signal of a voltage-controlled oscillator and

also subjected to a mixing with a local oscillator signal and optionally a modulation, and the output signals of which, after transmission by way of a charge pump device and a passive loop low-pass filter, are provided for controlling the voltage-controlled oscillator, wherein for setting (precharge) a certain initial state of the voltage-controlled oscillator, used for a rapid "lock-in", the charge pump device is controlled during the transient phase in such a way that it ensures the supply of the control voltage, respectively necessary for the initial state, at the voltage-controlled oscillator,

wherein a precharge function is integrated into the charge pump device in such a way that in each case a multiplexer is arranged between each of the two outputs of the phase-frequency detector and each of the two inputs of the charge pump,

wherein to perform the precharge function the charge pump device is activated by two logic control signals, wherein the one logic control signal ensures that during the precharge the phase-locked loop is in the standby mode and only the charge pump with precharge function is in the active mode, and after the precharge the PLL phase-locked loop is in the active mode, and in that the other logic control signal, which is supplied to the one multiplexer directly and to the other multiplexer by way of an inverter, so that the output signals of the phase-frequency detector are linked to this control signal or to the control signal inverted with respect to it, with the result that it is ensured that the charge pump applies to the voltage-controlled oscillator the control voltage respectively necessary for the initial state.

Advantageous developments of the invention are set out in claims 2 to 6.

The PLL phase-locked loops designed according to

the invention are assembled advantageously in integrated circuit technology (IC).

For a better understanding of the present invention, and to show how it may be brought into effect, reference will now be made, by way of example, to the accompanying drawings, in which:

Figure 1 shows the block diagram of a known PLL frequency synthesizer with loop mixer (MPLL), already explained in the introduction to the description.

Figure 2 shows the block diagram of an up-conversion modulation loop transmitter (UML-TX) which is likewise known and is already explained in the introduction to the description.

Figure 3 shows an already explained timing diagram for a "software-precharge" in the known circuits according to Figures 2 and 3.

Figure 4 shows the block diagram of a PLL frequency synthesizer with loop mixer (MPLL) and precharge pump provided in accordance with the invention.

Figure 5 shows a timing diagram for the precharge pump of the circuit according to Figure 4.

Figure 6 shows the block diagram of a PLL frequency synthesizer with loop mixer (MPLL) and a precharge constructed according to a variant of the invention.

In Figure 4, with the aid of a PLL frequency synthesizer with loop mixer (MPLL) the new precharge concept according to the invention for such PLL phase-locked loops is shown. The PLL phase-locked loop corresponds closely with that shown in Figure 1, so that an explanation of the corresponding parts can be dispensed with here.

However, in the circuit according to Figure 4, in addition a precharge pump 11 is inserted parallel to the charge pump 9. Although in Figure 4 only the MPLL

phase-locked loop with precharge pump 11 is shown, this concept applies to all other PLL phase-locked loops, for example PLL and UML-TX (basic block diagram is shown in Figure 2).

The precharge pump 12 consisting of two current sources "source" and "sink" and an inverter 11 is activated by two signals pcp and pd. If, for example, pd = low, the PLL phase-locked loop (PPL) is then in the standby mode and only the precharge pump 12, which is activated by the signal pd by way of an inverter 13, is in the active mode. The control signal pcp can be programmed with the aid of software or hardware. When pcp = high, the current source "source" of the precharge pump 11 is connected, and as output voltage for controlling the voltage-controlled oscillator (VCO) 2 Vcp = Vcc is obtained for $f_{LO} = f_{RF} + f_{IF}$ (GSM).

When pcp = low, by way of the inverter 11 the current source "sink" of the precharge pump 12 is connected. Then Vcp = gnd(0) is for $f_{LO} = f_{RF} - f_{IF}$ (PCN and PCS). After the precharge the PLL phase-locked loop is changed over into the active mode and the precharge pump 12 into the standby mode (pd = high).

Figure 5 shows a simplified timing diagram of the precharge pump 12 without and with band change (single and dual band applications). The control signals pcp and pd can be programmed with hardware or software. By means of the omission of the two separate programming procedures with software, necessary in the hitherto-existing solutions, in this respect the timing for the precharge is uncritical. The period t_{PCP} is called precharge time. In Figure 3 Vcc represents the supply direct voltage, Vcp the control voltage for the voltage-controlled oscillator (VCO) 2 and gnd the earth potential.

The precharge pump 12 can be implemented with simple voltage-controlled or current-controlled current

sources in bipolar or/and CMOS transistors because only small demands are made of the speed and accuracy in comparison with the charge pump 9 in the PLL phase-locked loop. The precharge duration depends on the current variable I_{PCP} of the precharge pump 12 and the elements of the passive loop low-pass filter 10.

For this reason the precharge duration can be shortened by an optimization of the precharge pump 12 and the passive loop low-pass filter 10. The precharge takes place in the standby mode of the PLL phase-locked loop and therefore can be implemented with simple circuits, and so the power consumption during the precharge is substantially reduced.

For single band applications the output voltage Vcp can be established after the precharge or the precharge polarity can be established after initialization (1. programming after power-on), i.e. no additional programming of the precharge before the active mode is necessary. In this way, the operating time of the PLL phase-locked loops can be reduced. However, it is necessary for the precharge current I_{PCP} to be reduced for this purpose so that the entire power consumption in the standby mode is acceptable.

According to an alternative design, the precharge function can also be implemented with the existing charge pump 9 of the PLL phase-locked loops, as is shown in the block diagram of Figure 6. In Figure 6 this alternatively designed new precharge concept according to the invention is likewise shown with the aid of a PLL frequency synthesizer with loop mixer (MPLL) for such PLL phase-locked loops.

The PLL phase-locked loop corresponds widely with the one shown in Figure 1, so that here also an explanation of the corresponding parts can be dispensed with. However, in a specially constructed charge pump device 14 with precharge function two 2:1 multiplexers

(Mux) 15 and 16 are inserted in front of the actual charge pump 9, so that the outputs of the phase-frequency detector (PFD) 4 are linked to the control signal pcp or to the control signal pcp inverted by means of an inverter 17 and so that in the standby mode of the PLL phase-locked loops the charge pump 9 with precharge function can remain in the active mode.

The charge pump 9 of the phase-locked loops (PLL) is normally assembled with circuit engineering which is more accurate and faster than the precharge pump 12 according to Figure 5, and so the power consumption of the alternative concept according to Figure 6 during the precharge is higher than with the precharge according to the design of Figure 4, described first of all.

The two new precharge designs explained with reference to Figure 4 and Figure 6 have the following advantages compared with the hitherto-existing software precharge.

1) There is only a low power consumption during the precharge because only the precharge pump 12 in Figure 4 or the charge pump device 14 with precharge enclosed therein in Figure 6 is in the active mode.

2) The timing for the precharge is not critical as a result of the omission of the two separate programming procedures with software.

3) For single-band and dual-band applications without band change the programming procedure for the precharge is omitted, with the PLL phase-locked loops being connected quickly as a result.

CLAIMS

1. Phase-locked loop for high-frequency signals with a phase-frequency detector to which there is supplied, as one input signal, a reference signal generated by way of frequency division, as second input signal likewise generated by way of frequency division a signal derived from the output signal of a voltage-controlled oscillator and also subjected to a mixing with a local oscillator signal and optionally a modulation, and the output signals of which, after transmission by way of a charge pump device and a passive loop low-pass filter, are provided for controlling the voltage-controlled oscillator, wherein for setting (precharge) a certain initial state of the voltage-controlled oscillator, used for a rapid "lock-in", the charge pump device is controlled during the transient phase in such a way that it ensures the supply of the control voltage, respectively necessary for the initial state, at the voltage-controlled oscillator,

wherein the charge pump device, in addition to the charge pump, also contains a precharge pump which is activated by two logic control signals,

wherein the one logic control signal ensures that during the precharge the phase-locked loop is in the standby mode and only the precharge pump is in the active mode and after the precharge, conversely, the phase-locked loop is in the active mode and the precharge pump is in the standby mode, and wherein the other logic control signal ensures that the precharge pump applies to the voltage-controlled oscillator the control voltage respectively necessary for the initial state.

2. Phase-locked loop according to claim 1, wherein the logic control signals are programmed by hardware.

3. Phase-locked loop according to claim 1, wherein the logic control signals are programmed by software.

4. Phase-locked loop according to any preceding claim, wherein the precharge pump is designed in the form of two simple voltage-controlled or current-controlled current sources (source, sink) with bipolar and/or CMOS transistors.

5. Phase-locked loop according to one of claims 1-4, wherein the precharge pump and the loop low-pass filter are designed with respect to their power consumption in such an optimized manner that a shortened precharge duration results.

6. Phase-locked loop according to one of the preceding claims, wherein for single-band applications the control voltage to be supplied to the voltage-controlled oscillator is established after the precharge or the precharge polarity is established after initialization, i.e. of the first programming after the power-on, so that no additional programming of the precharge before the active mode is necessary, and in that the precharge current I_{PCP} is reduced for this purpose so that the entire power consumption in the standby mode is relatively small.

7. Phase-locked loop for high-frequency signals with a phase-frequency detector to which there is supplied, as one input signal, a reference signal generated by way of frequency division, as second input signal likewise generated by way of frequency division a signal derived from the output signal of a voltage-controlled oscillator and also subjected to a mixing with a local oscillator signal and optionally a modulation, and the output signals of which, after transmission by way of a charge pump device and a passive loop low-pass filter, are provided for controlling the voltage-controlled oscillator, wherein

for setting (precharge) a certain initial state of the voltage-controlled oscillator, used for a rapid "lock-in", the charge pump device is controlled during the transient phase in such a way that it ensures the supply of the control voltage, respectively necessary for the initial state, at the voltage-controlled oscillator,

wherein a precharge function is integrated into the charge pump device in such a way that in each case a multiplexer is arranged between each of the two outputs of the phase-frequency detector and each of the two inputs of the charge pump,

wherein to perform the precharge function the charge pump device is activated by two logic control signals, wherein the one logic control signal ensures that during the precharge the phase-locked loop is in the standby mode and only the charge pump with precharge function is in the active mode, and after the precharge the PLL phase-locked loop is in the active mode, and in that the other logic control signal, which is supplied to the one multiplexer directly and to the other multiplexer by way of an inverter, so that the output signals of the phase-frequency detector are linked to this control signal or to the control signal inverted with respect to it, with the result that it is ensured that the charge pump applies to the voltage-controlled oscillator the control voltage respectively necessary for the initial state.

8. A phase-locked loop substantially as herein described with reference to Figs 4-6 of the accompanying drawings.

9. Phase-locked loop according to one of the preceding claims, formed in integrated circuit technology.

10. An integrated circuit having a phase-locked loop as claimed in claim 9.

Application No: GB 9913096.5
Claims searched: ALL

Examiner: Mr.Sat Satkurunath
Date of search: 25 August 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H3A: AXC, AXX

Int Cl (Ed.6): H03L

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	US 5523724	ASSAR - see especially figures 7-9	1, 7
A	US 5220294	ICHIKAWA - see especially abstract and figure 4	1, 7

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

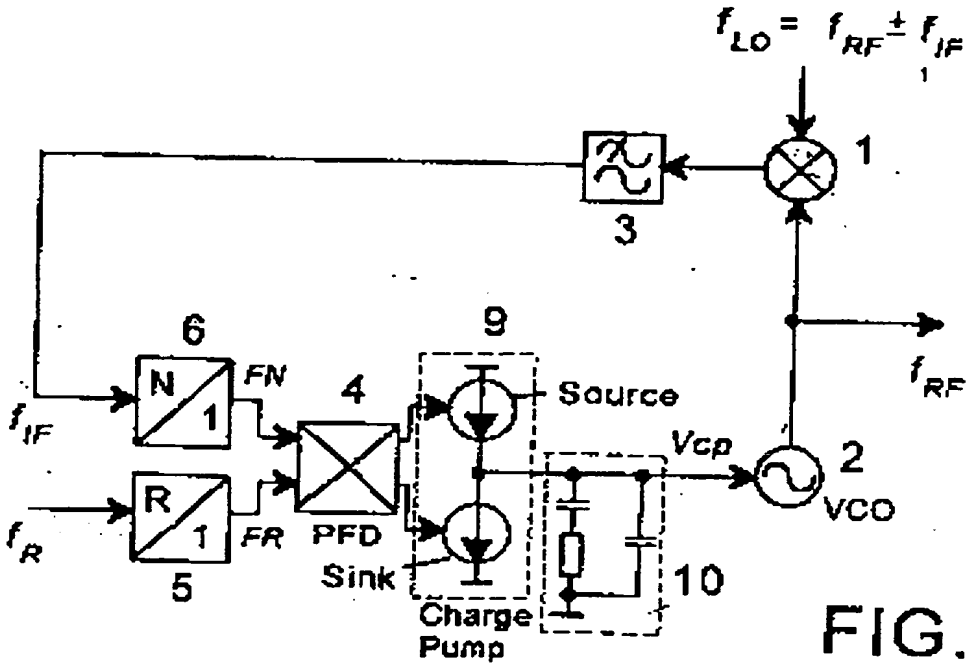

FIG. 1

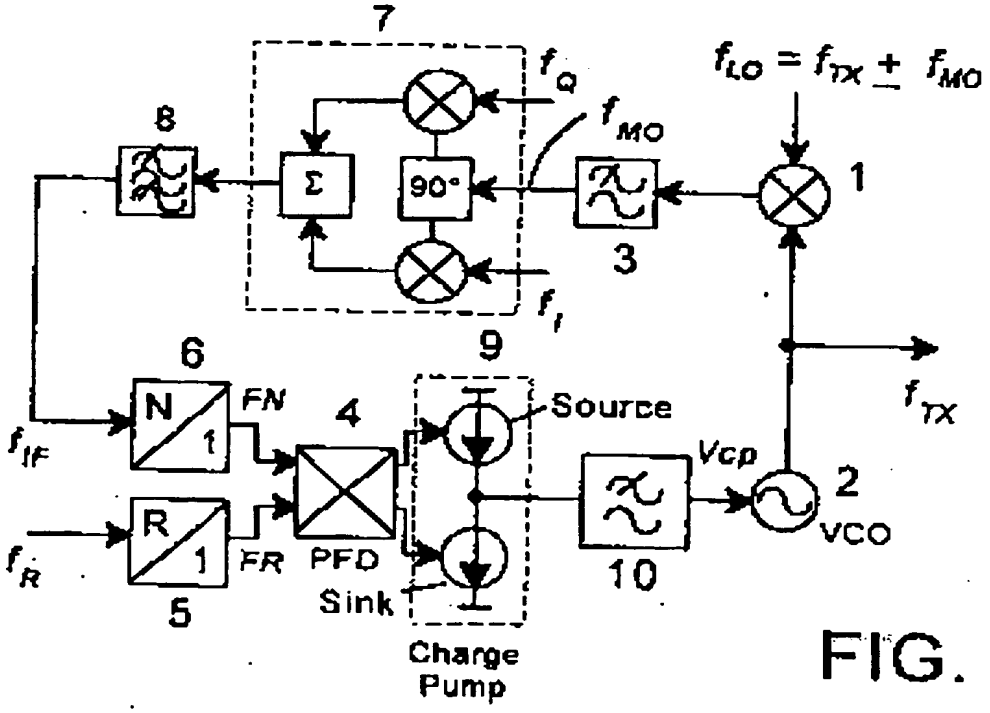

FIG. 2

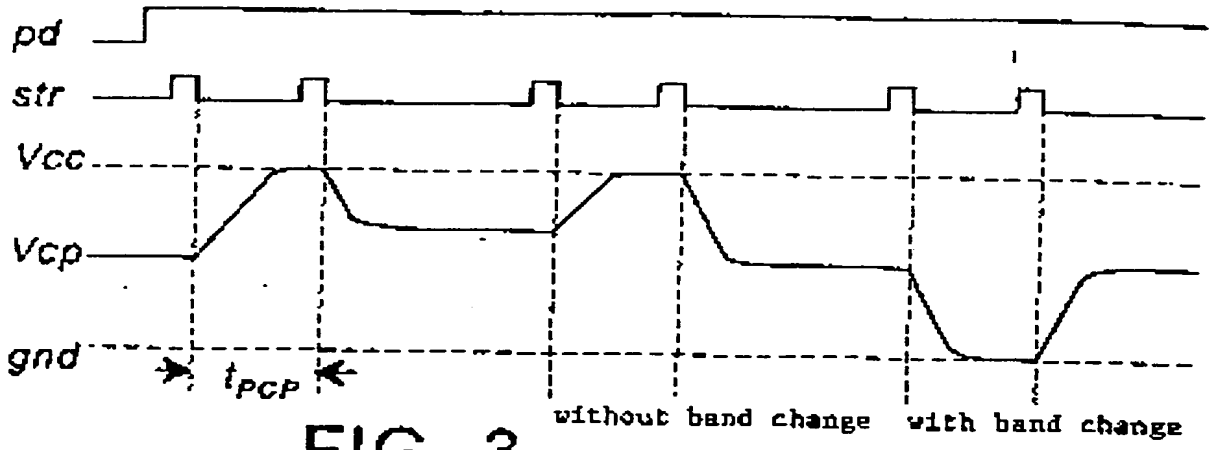

FIG. 3

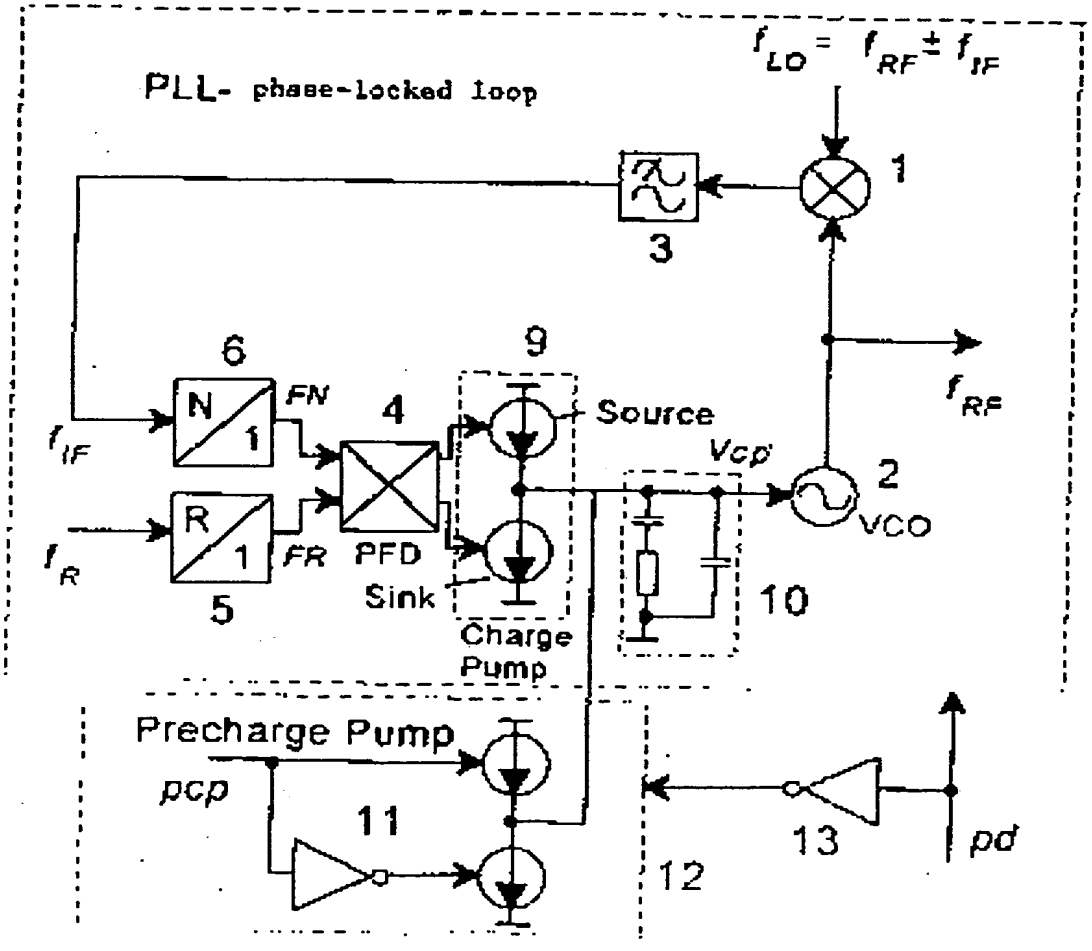

FIG. 4

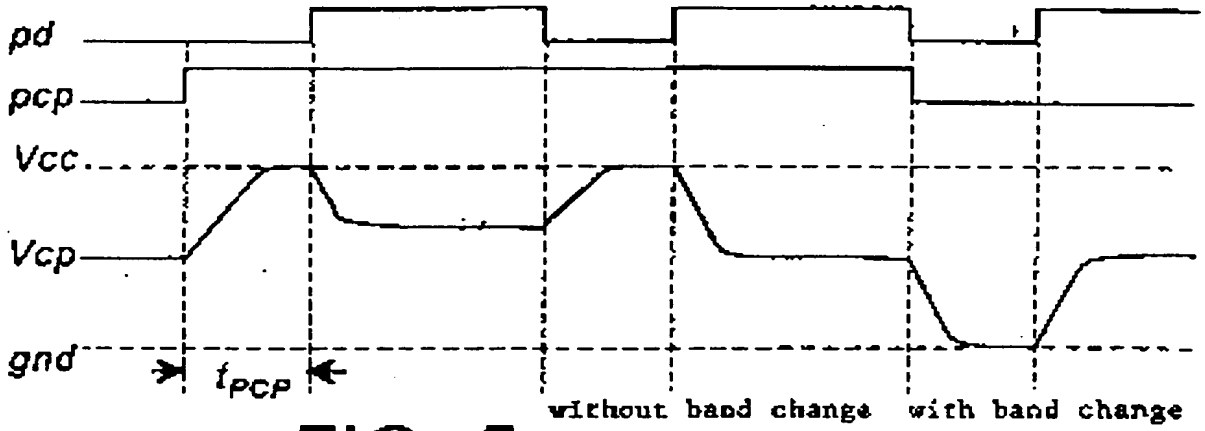

FIG. 5

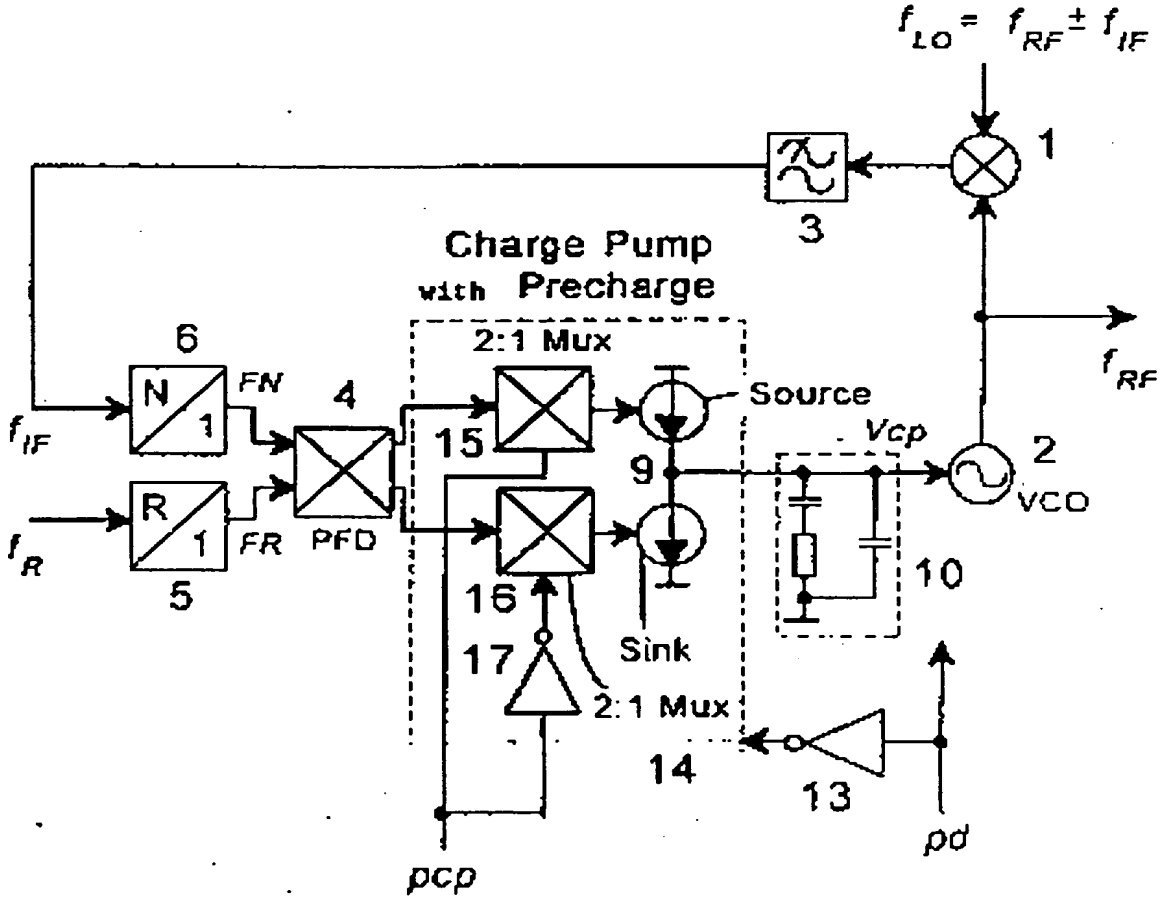

FIG. 6

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